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(71) Applicant: **DELCO ELECTRONICS CORPORATION**
700 East Firmin Street
Kokomo Indiana 46902(US)

(72) Inventor: **Koslak, Walter Kirk**
2717 South Park Road
Kokomo, Indiana 46902(US)
Inventor: **Mann, Jonathan Douglas**
556 Kokomo Regency
Kokomo, Indiana 46902(US)
Inventor: **Rowlands, Paul Russell, III**
2204 Rouge Drive
Kokomo, Indiana 46902(US)
Inventor: **Schnabel, Douglas Robert**
3204 Woodbridge Circle
Kokomo, Indiana 46902(US)
Inventor: **Parrish, Jack Duana**
813 Williamsburg Drive
Kokomo, Indiana 46902(US)

(74) Representative: **Haines, Arthur Donald et al**
Patent Section Vauxhall Motors Limited 1st Floor Gideon House 26 Chapel Street
Luton, Bedfordshire LU1 2SE(GB)

## (54) Process for forming high-voltage and low-voltage CMOS transistors on a single integrated circuit chip.

(57) A process for forming both low-voltage CMOS transistors and high-voltage CMOS transistors on a common integrated circuit chip uses a common implantation and drive-in step to form both the n-type well (174,374) of each PMOS transistor and the n-type drain extension well (274) of each lightly-doped drain (LDD) NMOS transistor and a separate implant and drive-in to form the p-type drain extension well (182) of each LDD PMOS transistor.

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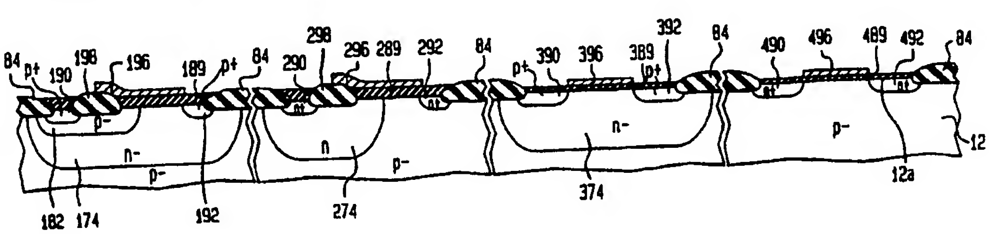
FIG. 2I



# PROCESS FOR FORMING HIGH-VOLTAGE AND LOW-VOLTAGE CMOS TRANSISTORS ON A SINGLE INTEGRATED CIRCUIT CHIP

## Field of the Invention

This invention relates to the manufacture of complementary metal-oxide-semiconductor (CMOS) integrated circuits as specified in the preamble of claim 1, for example as disclosed in "Enhanced CMOS for Analog-Digital Power IC Applications" by G.M.Dolny et al, IEEE Transactions on Electron Devices, Vol.ED-33 No.12, pages 1985-1991 (December 1986).

## Related Applications

This patent application is related to European patent application Number corresponding to USSN 325 164, and entitled "Process for Forming Vertical Bipolar Transistors and High Voltage CMOS in a Single Integrated Circuit Chip," which is being filed concurrently with the present European patent application.

## Background of the Invention

CMOS integrated circuits are finding increased use in electronic applications. There are at least two important classes of CMOS integrated circuits, low-voltage circuits in which the operating voltages are no greater than about six volts and high-voltage circuits in which the operating voltages are above about thirty volts. Moreover, an important difference in the two classes is that the higher operating voltages require that the channel region between the source and drain of the higher voltage MOS transistor be able to withstand the higher induced electric field without experiencing avalanche breakdown. As a consequence, the two classes have generally involved differences in form, as well as differences in parameters. Such differences have dictated enough differences in processing that each class typically has been formed in its own separate chip rather than combined with the other class in a common chip.

However, it is advantageous to have a process for forming both types in a common chip, or monocrystalline substrate, and processes have been proposed to this end.

However, such processes are generally quite complex and require considerable change from established processes.

There is desired an improved process for forming both high-voltage CMOS and low-voltage CMOS devices in a common chip that involves only a few changes in an established process for making the more common low-voltage CMOS devices.

One favoured form for realizing higher avalanche breakdown voltages to the field induced between the source and drain of an MOS transistor is lightly-doped drain (LDD) structure in which the drain includes a lightly-doped extension portion intermediate between the channel region and the standard heavily-doped drain portion.

Additionally, in a high-voltage MOS transistor, it is usually advantageous to include a gate oxide whose thickness, typically at least 65 nm (650 angstroms), is thicker than that normally used in a low-voltage MOS transistor, typically no greater than about 40 nm (400 angstroms). Such added thickness provides ruggedness that serves as added assurance against electrical over-stress (eos) of the gate oxide layer.

## Summary of the Invention

A process according to the present invention is characterised by the features specified in the characterising portion of claim 1.

The present invention is directed to a process for providing both high-voltage and low-voltage CMOS devices in a common chip that basically involves adding a single ion implantation step, some non-critical masking and mask design changes to an established n-type well, low-voltage CMOS integrated circuit process.

In particular, early in this novel process, the mask that [illegible] characteristically used with the standard donor [illegible] implantation step for forming in a p-type substrate n-type wells for the p-channel (PMOS [illegible] is modified additionally to form extension [illegible] wells for the high-voltage n-channel (NMOS [illegible]. Additionally, the novel process in[illegible] added acceptor ion implantation step for [illegible] wells for use in forming the high-voltage [illegible] transistors. In particular, the parameters [illegible] implantation step that forms the p-type [illegible] well permits the standard field oxidation step [illegible] used to drive-in the implanted ions.

Moreover, in a preferred embodiment for achieving additionally a thicker gate oxide layer in each of the high-voltage transistors, at an intermediate stage in the process, a mask used for localizing an oxide-etching step is modified to protect the oxide in the active region of each high-voltage transistor so that ultimately the gate oxide

layer of each high-voltage transistor is thicker than that of each low-voltage transistor.

Th invention will be better und rstood from the following more detailed description taken in conjunction with the appended claims and with the accompanying drawings.

## Brief Description of the Drawings

Fiqures 1A, 1B, 1C and 1D are cross-sections of known forms of a high-voltage PMOS transistor, a high-voltage NMOS transistor, a low-voltage PMOS transistor and a low-voltage NMOS transistor, respectively, all sharing a common substrate for processing in accordance with the invention in a common substrate; and

Figures 2A, 2B, 2C, 2D, 2E, 2F, 2G, 2H and 2I are cross-sections of a substrate at selected stages, as it is being processed in accordance with an illustrative embodiment of the present invention to include one of each of the four transistor forms shown in Fiqures 1A, 1B, 1C and 1D.

It is to be noted that the drawings are not true to scale. Moreover in the drawings, heavily-doped regions (concentration of impurities of at least about 1 x $10^{19}$ impurities/cm$^3$) are designated by a plus sign (e.g., n+) and lightly-doped regions (concentrations of no more than about 5 x $10^{15}$ impurities/cm$^3$) by a minus sign (e.g., p-).

## Detailed Description

Referring now to Figure 1A, there is shown a known form of a high-voltage PMOS transistor 10 of the lightly-doped drain (LDD) type included entirely in a lightly-doped n-type well 11 that is formed in a lightly-doped p-type substrate 12. Nested within the n-type well 11 is a lightly-doped p-type well 14 that serves as the lightly-doped drain extension characteristic of an LDD PMOS transistor. Heavily doped p-type region 16 in well 14 serves as the standard drain of the transistor. Heavily doped p-type region 18 in well 11 serves as the source of the transistor.

Relatively thick field oxide regions 20 at a top surface 12a of substrate 12 define the ends of the active surface region of transistor 10 and serve to isolate it from other transistors at the surface of the substrate 12. Generally, such regions are predominantly of silicon dioxide but are conventionally describ d as of "oxide" or "silicon oxid " and will be so term d her aft r. Moreover, other layers used in the process of the invention that will be termed "oxide" or "silicon oxide" lay rs g n rally also are layers predominantly of silicon dioxide.

A region 21 of thick field oxid is also optionally included over an intermediate region of the p-well 14. A relatively thin silicon oxide layer 22 serves as th gate dielectric and extends over surface 12a from an edge of the p-type source 18 to region 21 of the field oxide. A polysilicon gate electrode 24 extends over the gate oxide layer 22 and overlaps a portion of the field oxide region 21. Such an overlap is known to permit the gate electrode 24 to serve also as a quasi-field plate to improve the breakdown characteristics of the transistor.

In a typical embodiment designed to have a threshold voltage of about -0.85 volts and an avalanche breakdown voltage of at least minus thirty volts, the substrate 12 has an average acceptor concentration of about 5 x $10^{15}$ impurities/cm$^3$ to provide a resistivity of around 18 ohms-cm, the gate oxide layer 22 is about 65 nm (650 angstroms) thick; the channel between p-well 14 and p-type source 18 is about 4 micrometres long; the portion of the p-well 14 that extends under the gate electrode 22 before it starts to overlap the field oxide region 21 is about 1 micrometre long and the length of the gate electrode overlap of the field oxide region 21 is about 2 micrometres. The source and drain are each doped to about 1 x $10^{19}$ impurities/cm$^3$ and are about 0.3 micrometres deep. The n-well 11 is about 4 micrometres deep and has an average concentration of about 1 x $10^{16}$ impurities/cm$^3$, and the p-well 14 has an average concentration of about 4 x $10^{16}$ impurities/cm$^3$ and is about 1 micrometre deep.

Referring to Figure 1B, there is shown a high-voltage NMOS transistor 30 of the LDD type which includes the p-type substrate 12 within which is formed a lightly-doped n-type well 32 that serves to provide the characteristic lightly-doped drain extension. Within it there is formed a standard heavily-doped n-type drain 34. Heavily-doped n-type region 36 at the surface 12a in the p-type substrate 12 serves as the source. Thick field oxide regions 38 define the active surface region of the transistor 30. A thin gate oxide layer 40 overlies the surface 12a and extends to an intermediate thick field oxide region 39 that extends between the drain 34 and the end of the gate oxide layer 40. A polysilicon gate electrode 42 extends over the gate oxide layer 40 and overlaps a thick field oxide portion 39, as in the LDD PMOS transistor of Figure 1A, to serve also as a quasi-field plate.

To make the processing of this LDD NMOS transistor 30 compatible with the processing of the LDD PMOS transistor 10 of Figure 1A, the basic parameters of the substrate 12, the thicknesses of the gat oxide lay rs 22 and 40, and the doping and depth of n-type wells 11 and 32 are made the same in the two transistors. Additionally, in transistor 30 the n-typ source 36 and drain 34 ar doped

to an average concentration of 1 x $10^{20}$ donors/$cm^3$ and are about 0.3 micrometres deep. The length of the channel between the n-type source 36 and the n-type extension well 32 is about 7 micrometres and the various dimensions of gate electrode overlaps are the same as in the PMOS transistor 10. In transistor 30, the threshold voltage is about 1.4 volts and the avalanche breakdown voltage is at least 30 volts.

Referring now to Figure 1C, there is shown a conventional low-voltage PMOS transistor 50 which includes as before the p-type substrate 12 in which is formed a lightly-doped n-type well 52. A heavily-doped p-type source 54 and drain 55 are spaced apart within the n-type well 52. Gate oxide layer 57 and polysilicon gate electrode 58 overlie the portion of surface 12a lying between the source 54 and drain 55 in the fashion characteristic of a PMOS transistor. Thick field oxide regions 59 define the ends of the active surface region of the transistor 50.

For compatibility of processing, the doping of the source 54, drain 55, substrate 12 and n-type well 52 are the same as those of the corresponding elements of LDD PMOS transistor 10 shown in Figure 1A. The length of the channel between source 54 and drain 55 is also about 1.5 micrometres and the thickness of the gate oxide in this low voltage transistor is about 40 nm (400 angstroms) to provide a threshold voltage of -0.75 volts. The avalanche breakdown voltage is at least about -15 volts.

Referring now to Figure 1D, there is shown a conventional low-voltage NMOS transistor 60. It, too, is formed in lightly-doped p-type substrate 12 and includes heavily-doped n-type source 62 and heavily-doped n-type drain 64 which are spaced apart at the surface 12a. A thin gate oxide layer 65 and a polysilicon gate electrode 66 overlie the channel between the source 62 and the drain 64 in characteristic fashion. Thick field oxide regions 68 define the ends of the active surface region of transistor 60.

For compatibility in processing, the doping of the source 62, drain 64, and substrate 12 of transistor 60 are similar to those corresponding elements of the LDD NMOS transistor shown in Figure 1B, and the gate oxide layer 65 has the thickness of gate oxide layer 57 of the complementary PMOS transistor 50 shown in Figure 1C. The length of the channel of transistor 60 is 1.5 micrometres. The threshold voltage and the avalanche breakdown voltag of transistor 60 ar +0.75 volts and +10 volts, respectively.

As previously indicated, the invention is primarily a process for forming efficiently the four forms of transist rs, shown in Figures 1A, 1B, 1C and 1D, in a common substrate, so that there may b provided individual chips that include one or more of each of the four forms for use in a monolithic integrated circuit. Howev r, if desired,. after processing the four forms in a common substrate, the substrate may be diced in a fashion to provide individual chips that include less than all four forms.

Typically, in such a monolithic integrated circuit, the low-voltage transistors are used at the logic and intermediate stages for signal processing, while the high-voltage transistors are used at input and output stages of an integrated circuit. Such an integrated circuit is expected to be particularly useful for driving vacuum fluorescent displays or automatic data buses. Additionally, such an integrated circuit makes it possible for logic level voltage supplies to be derived from an on-chip voltage regulator circuit.

Of course, a variety of other functions can be provided advantageously by an integrated circuit that includes both high-voltage and low-voltage CMOS pairs of transistors.

It is appropriate now to describe an illustrative embodiment of the process of the invention.

Referring now to Fiqure 2A, there is shown a lightly-doped p-type substrate 12 in which one of each of the transistors shown in Figures 1A, 1B, 1C and 1D is to be formed. Substrate 12 is a portion of a monocrystalline silicon wafer that has been cut so that its top surface 12a lies along a < 100 > crystal plane, as is usual in MOS technology. The wafer of which the substrate 12 is part is made just thick enough to be handled conveniently, typically between 584.2 and 660.4 micrometres (23 and 26 mils). The lateral dimensions of the wafer being processed are generally large enough so that the wafer may subsequently be diced into a number of chips, each of which includes one or more transistors of the kind described. However, the figures will focus on a substrate portion that includes just one of each.

The processing begins by providing donor-implanted surface regions 171, 271 and 371 spaced apart in the substrate 12, as shown in Figure 2A, that will be used to form n-type wells. To this end, a layer of silicon oxide thick enough to be a barrier (about 550 nanometres thick) is first thermally formed on the top surface 12a of the substrate 12. Then, by use of photolithography, this oxide layer is patterned to bare each of those portions of the top surface 12a of the silicon substrate 12 where an n-type well is to be included. Then the substrate 12 is treated to form a layer of thinner oxide (e.g., 50 nanometres) over the bared silicon portions. These thin oxide layer portions are design d primarily to protect the surface 12a of the silicon substrate 12 during the subs quent ion implantation without significantly blocking the implantation.

while the thicker layer portions are intended to block such implantation into the underlying regions of the substrate 12.

The wafer is then implanted with th donor ions to form ion-implanted regions localized at surface portions underlying the thin oxide layer portions. Typically the implantation is of phosphorus at an accelerating voltage of about 125 KeV to a dosage of 4.5 x $10^{12}$ ions-cm$^{-2}$. Advantageously, the implantation is done in known fashion at an angle from the normal to minimize channelling effects.

The result is shown in Figure 2A where the top surface 12a of the substrate 12 includes layer portions 170a, 270a, 370a and 470a of thick oxide and layer portions 170b, 270b and 370b of thin oxide and donor-implanted regions 171, 271 and 371 underlying the thin oxide layer portions 170b, 270b and 370b, respectively. Arrows 72 denote the ions being implanted.

Additionally, as is discussed more fully in the above-identified related European application, a vertical n-p-n bipolar transistor may optionally be formed in the common substrate with essentially no additional steps. In such an instance, a fourth n-type well would be formed in the substrate by the same implantation used to form the three n-type wells shown. This fourth well would serve as the collector of the vertical n-p-n transistor.

Next, the substrate 12 is heated to drive the phosphorus ions deeper into the substrate 12 and form n-type wells therein. Typical heating conditions are 1200° C. for 4 hours. Then the substrate 12 is treated to clean off the oxide layers on the top surface of the substrate. There then results the structure shown in Figure 2B where the phosphorus-implanted regions have formed the n-type wells 174, 274 and 374.

Next, as shown in Figure 2C, there is formed an acceptor-implanted region 175 nested selectively within n-well 174 that will serve, after drive-in, as the p-type drain extension well in the high-voltage PMOS transistor. To this end, a protective oxide layer 76, typically 50 nanometres thick, is grown over the top surface of the substrate, and a masking layer of photoresist (not shown) deposited over it. The photoresist is then patterned to expose the underlying protective oxide layer where region 175 is to be formed, but elsewhere it is left as a mask to block the acceptor implantation. Boron is then implanted selectively to form the region 175. Illustratively, the boron is implanted at 120 KeV at a dosage of 1.5 x $10^{13}$ ions-cm$^{-2}$. By this choice, advantageously, the drive-in of the boron to form the p-type drain ext nsion well can be postponed and made to occur during th h ating step used subsequently to form the thick field oxide regions.

Moreover, if a vertical n-p-n transistor is to be formed in the substrat as mentioned above, the boron implantation step is also used to form a boron-implanted region in the fourth n-type well that can b used to form the p-type bas of the n-p-n vertical transistor.

To provide the various thick field oxide regions, a mask is first formed over the top surface 12a of the substrate 12 to localize the oxidation as desired.

To this end, a layer, illustratively of silicon nitride about 200 nanometres thick, is formed over the thin oxide layer 76 by the usual low pressure chemical vapor deposition (LPCVD) process. This nitride layer is then patterned photolithographically in the usual fashion to remove the nitride where thick field oxide regions are desired, leaving the mask formed by regions 178, 278, 378, and 478 of silicon nitride, seen in Figure 2D.

Moreover, it is usually advantageous to ensure against undesirable surface inversion effects in the substrate 12 under the thick field oxide regions. For this purpose, it is the usual practice to implant acceptor ions selectively in the p-type surface 12a portions of the substrate 12 that underlie the thick field oxide regions. To this end, a layer of photoresist that is then patterned to form the mask 80 is provided over the silicon nitride mask, as seen in Figure 2D. This mask 80 leaves exposed surface regions that are not included within any of the n-type wells nor covered with silicon nitride. The substrate 12 is then implanted with boron, denoted by arrows 81 in Figure 2D, illustratively at a dosage of 1.4 x $10^{13}$ ions-cm$^{-2}$ at an accelerating voltage of 35 KeV. The low accelerating voltage results in a very shallow implant. To keep the drawing simple, the effect of this implantation in the composition of the substrate 12 is not reflected in Figure 2D and the subsequent figures, since only the concentration of impurities, and not the conductivity type of the substrate, is affected.

After this implantation step, the photoresist mask 80 is removed to expose the patterned silicon nitride 178, 278, 378 overlying the surface 12a of the substrate 12. The substrate 12 is then heated at a temperature of 1050° C. for about 4 hours to form the desired thick field oxide regions, typically about 850 nanometres thick, over the portions of the surface 12a not protected by the patterned silicon nitride. This heating step also serves to drive-in the boron implanted in region 175 to form a p-type extension well 182 (see Figure 2E) in n-type well 174.

Next, the top surface 12a of the substrate 12 is bared of all but the thick field oxide regions. To this end, th oxide form d over th silicon nitride mask during the fi ld oxidation, the silicon nitride mask, and finally the thin oxide that was under the silicon nitride mask are removed, usually in turn. The thicker field oxide regions normally are little af-

fected by these steps. The resultant is seen in Figure 2E where p-typ ext nsion well 182 is nested in n-type well 174 and thick oxide regions 84 are seen formed where needed over the surfac of the substrate to define the ends of the active surface areas of the various transistors and to form the intermediate oxide regions used to form the quasi-field plates in the LDD types of transistors seen in Figures 1A and 1B.

Next, a thin layer of oxide, illustratively about 40 nanometres thick, is grown over the portions of the surface of the silicon substrate 12 that are exposed between the thick oxide regions 84. This is then advantageously followed by a light and shallow implant of boron ions over the regions of the substrate corresponding to the future active regions of the transistors to set the surface potential of the active surfaces of the transistors and to adapt such surfaces better for the enhancement mode transistor operation, typical of the transistors formed by the process of the invention. An illustrative dosage is 1.35 x $10^{12}$ ions-$cm^{-2}$ at an accelerating voltage of 35 KeV. The effect of this implantation step also is not reflected in the figures since it affects only surface concentration and not surface conductivity type of the substrate 12.

As previously mentioned, in the preferred embodiment of the invention being described, the high-voltage transistors advantageously are provided with thicker gate oxide layers than are the low-voltage transistors. To this end, a layer of photoresist useful for masking is then deposited over the top surface 12a of the substrate 12 and selectively removed from the regions corresponding to the active surface areas of the low-voltage PMOS and NMOS transistors to bare the just-formed thin silicon oxide layer over such areas. This bared thin oxide layer is then selectively removed from the regions corresponding to the active surface areas of the low-voltage transistors.

The resultant is shown in Figure 2F in which patterned photoresist layer 86 masks the portion of the substrate 12 that will house the high-voltage CMOS transistors and thus has protected the thin oxide layer 88 previously formed over the active regions of these transistors. Over the surface regions where the low-voltage transistors are to be formed, there is no photoresist mask and the previously formed thin oxide layer is now absent.

Now the formation of the gate oxide layers can be completed. To this end, the remainder of the photoresist layer 86 is removed. Then the substrate 12 is again exposed to an oxidizing ambient atmosphere at an elevated temperature to grow a fresh oxide layer about 40 nanometres thick over the bare surface 12a areas where the low voltage transistors are to be formed and also to thicken the pre- xisting 40 nanometres oxide layer 88 that remains where the high voltage transistors are to be formed.

In some instances, since the first-formed thin oxide layer was exposed during the threshold implant and so is boron-rich, it may be preferably instead to remove completely said thin oxide layer before it is patterned. After its removal, there is grown a clean thin oxide layer over the substrate 12. This clean oxide layer is removed selectively where a thin gate oxide is desired. Then the additional oxidation step is used as before to grow a new thin oxide layer where the thinner gate oxide layer is desired and to thicken the clean oxide layer that remains where the thicker gate oxide layer is desired.

As is shown in Figure 2G, there now results the desired greater thickness in oxide layers 189 and 289, over the surface area where the high-voltage transistors are to be formed, than in oxide layers 389 and 489 over the surface areas where the low-voltage transistors are to be formed.

Next, a polysilicon layer that will provide the gate electrodes for all of the transistors is deposited over the top surface of the substrate 12 in any of the known ways. Typically, this involves low pressure chemical vapor deposition to form a polysilicon layer about 350 nanometres thick.

The polysilicon layer is generally doped to make it highly conductive, as is desired for its role as the gate electrode. Illustratively, this is done by heating the substrate 12 after the layer has been deposited, in an ambient atmosphere of phosphine gas in known fashion to saturate the polysilicon with phosphorus. Before the polysilicon layer is patterned to define the gate electrodes, it advantageously is de-glazed (etching away of the phosphosilicate layer formed on its surface during the doping step).

To pattern the polysilicon layer, typically it is coated first with a layer of photoresist and this photoresist layer is patterned to mask the polysilicon where the gate electrodes of the various transistors are to be formed. Then the exposed polysilicon is removed to leave only the polysilicon electrodes 196, 296, 396, and 496, seen in Figure 2H.

Next, the source and drain regions of the four forms of transistors are formed, illustratively by ion implantation using the polysilicon electrodes as masks to ensure proper alignment of the source and drains.

It is usual to form the heavily doped n-type source and drain regions before the heavily doped p-type source and drain regions. However, it is usually advantageous to form a temporary thin layer of oxide over the polysilicon electrodes to protect them during the subsequent processing.

However, before the implantation for the forma-

tion of these heavily-doped regions, a layer of photoresist is provided over the substrat 12, and this photoresist layer is patterned to open areas where the substrate 12 is to be implant d with donor ions to form the heavily-doped n-type regions that serve as the source and drains of the NMOS transistors.

Illustratively, these heavily-doped n-type regions are formed by a double implantation, first with arsenic at a dosage of 6.5 x $10^{15}$ ions-$cm^{-2}$ at an accelerating voltage of 100 KeV, and then with phosphorus at a dosage of 1 x $10^{14}$ ions-$c^{m-2}$ at an accelerating voltage of 70 KeV. this implantation is followed by a 15-minute anneal at 900° C.

Moreover, if a vertical n-p-n is to be formed, this implantation sequence is also used to form the emitter and a collector contact region of the vertical n-p-n transistor.

Next, the heavily-doped p-type sources and drains of the PMOS transistors are formed. To this end, a layer of photoresist is again formed over the substrate and then patterned to expose regions where the p-type sources and drains are to be formed by implantation of acceptor ions. For forming these, illustratively the substrate is implanted with boron fluoride ($BF_2$) at a dosage of 3 x $10^{15}$ ions-$cm^{-2}$ at an accelerating voltage of 70 KeV. After the implantation, the photoresist mask is cleaned off. Fiqure 2I shows the resultant. This represents the basic structure needed to provide the desired integration of low-voltage CMOS devices and high-voltage LDD CMOS devices in a common substrate.

Moreover, this boron implantation step also would be used to form a base contact region for a vertical n-p-n transistor.

As seen in Figure 2I, a high-voltage LDD PMOS transistor is formed in the n-type well 174. It includes the p-type extension well 182 within which is formed a p-type drain 190. A p-type source 192 is formed in the n-type well 174. The polysilicon gate electrode 196 overlies relatively thick oxide gate layer 189 and overlaps the intermediate field oxide region 198.

A high-voltage LDD NMOS transistor is formed in the p-type substrate 12 and includes n-type source 292 and n-type drain 290 included within n-type extension well 274. Polysilicon gate electrode 296 overlies relatively thick gate oxide layer 289 and also overlaps intermediate field oxide region 298.

A low-voltage PMOS transistor is formed in the n-type w ll 374 by p-typ source 390 and p-type drain 392. Polysilicon gate electrode 396 overlies relatively thin gate oxide lay r 389.

A low-voltage NMOS transistor is formed in the p-type substrat 12 by n-type source 492 and n-type drain 490 and polysilicon gate 496 overlying relatively thin gate oxide layer 489.

However, for use in a system, there remains the need to provide ohmic contacts to th various electrodes of the transistors. Also, there remains to be provided the various coatings, generally included for passivating and protecting the surfaces of the substrate 12, and the metal levels needed to interconnect the individual transistors into an integrated circuit.

Various known techniques are available for this further processing and the invention is not dependent on any particular such techniques.

However, an illustrative example of such further processing is as follows.

Proceeding further, the substrate is coated with a layer of phosphosilicate glass illustratively about 500 nanometres thick, followed by a short heating cycle at 900° C. for densification of the deposited glass in known fashion. Before depositing a metal contact layer, it is advantageous first to smooth the surface which has become substantially non-planar because of the stacking thereover of the various patterned layers.

Advantageously, this is done by spinning over the substrate 12 a layer of glass, typically a few hundred nanometres thick, to smooth its surface by filling any depressions at the surface. Advantageously, this is followed by heating to about 825° C. for about ten minutes in nitrogen, to densify the spun-on glass.

Then, to permit low-resistance ohmic contacts to be provided to the sources, drains and gate electrodes of the various transistors, contact openings are formed in the glass coatings where such contacts are to be provided.

To this end, the spin-on-glass (sog) layer is coated with a layer of photoresist that is then patterned to expose regions where there are to be formed contacts to the various sources, drains and gate electrodes through the glass layers.

Advantageously, to form well-defined contact openings with tapered sidewalls to facilitate good fill by the contact metal, the wafer is first treated with an isotropic wet etchant, such as aqueous hydrofluoric acid, and this is followed by an anisotropic dry plasma etch in known fashion.

Illustratively, the metal contacts are formed by first depositing over the surface a 600 nanometre thick layer of an aluminium-copper-silicon alloy (advantageously by weight about 98 parts aluminium, 1 part copper, 1 part silicon). This metal layer is then coated with a layer of photoresist that is patterned in known fashion to expose the metal layer where it is not n eded for the contacts desired, and this unneeded metal is then appropriately removed by a suitable techniqu .

It is also usual to provide a second level of metal to interconnect the various electrodes of the

transistors, as desired, and to provid bonding pads by which the int grated circuit device may be interconnected into a system. To this end, to provide _lectrical isolation between the first level metal already deposited and a second level metal to be deposited, a layer of silicon oxide, typically about 800 nanometres thick, is deposited over the surface of the substrate 12, illustratively by a plasma deposition process. The resulting surface, which tends to be non-planar, advantageously is made more planar, as before, by spinning a layer of glass, about 500 nanometres thick, over the surface and then etching most of it back to leave a substantially planar surface. Over this there is further deposited, typically by a plasma process, another layer of silicon dioxide about 400 nanometres thick.

Again, before deposition of the second level metal, access zones are formed in the various layers deposited to expose portions of the first level metal that are to be contacted by the second level metal. To this end, the top surface is again covered with a masking layer of photoresist that is then patterned to form openings where access zones are to be formed in the deposited layers. After the openings in the mask are formed, corresponding openings are formed in the layers of deposited oxide and the intermediate layer of spun-on-glass to expose the first level metal where contact to a second level is desired.

This is followed by deposition of the second level metal, which illustratively may be the same aluminium-copper-silicon alloy used for the first level metal. This second level metal is then appropriately patterned as desired.

Then, it is typical to deposit a layer of silicon nitride, generally by plasma-enhanced chemical vapor deposition (PECVD), over the surface of the wafer to protect the second level metal.

There finally remains the need to bare the second level metal where bonding pads are to be provided. This is typically done by first depositing a layer of photoresist over the surface that is then patterned to expose regions of the second level where the bonding pads are to be formed.

Finally, it is usually advantageous to heat the substrate 12 at about 425°C. for about an hour in a hydrogen-argon atmosphere to passivate the metals.

It is to be understood that the specific process described is merely illustrative of the general principles of the invention and that various changes may be made without departing from the scope of the invention as claim d. For example, there may be differences in the dimensions of the various layers and regions described. Additionally, there may be differences in the parameters of the various steps involved including differ nces in materials and dosages employed, as well as temperatures, times, and acc lerating voltages employ d. Moreover, in some instances, the particular order of the steps may obviously be changed without affecting the scope of the invention claimed.

The specific process described involved a p-type substrate as the bulk in which an n-type well was formed for use by each of the PMOS and high voltage NMOS transistors. Alternatively, an n-type substrate can be used as the bulk and a separate p-type well formed therein for use by each of the NMOS and high-voltage PMOS transistors. This would necessitate corresponding adjustment in the remainder of the processing.

Moreover, ordinarily the wafer will be eventually diced into chips, each of which includes one or more of each of the four different forms of MOS transistors that were processed in the wafer. However, in some instances, it may prove desirable to dice the wafer into some chips, for example, that include only the two high-voltage forms and separate chips that include only the low-voltage forms, and then to combine the two types of chips on a common printed circuit board or support for system use. This approach will still offer the benefit that both types of chips are processed in common on a single production line.

Moreover, while the preferred embodiment of the process included forming thicker gate oxide layers in the high-voltage devices, this is not a necessary feature of the invention and may be avoided.

Additionally, as is discussed in the above-identified related European patent application, the process may be readily adapted to provide additionally vertical bipolar transistors in the common substrate.

## Claims

1. A process for forming in a common substrate (12) of one conductivity type low-voltage transistors of said one type conductivity type and of the opposite conductivity type and high-voltage transistors of said one conductivity type and of the opposite conductivity type in which the high-voltage transistors of both types are of the lightly-doped drain type and include drain extension wells (182,274) and the transistors of said one conductivity type are formed in wells (174) of the opposite conductivity type <u>characterised in that</u>: the drain extension well (274) of the opposite conductivity type of each of the high-voltage transistors of the opposite conductivity typ is formed in common with the forming of the wells (374) of the opposit conductivity type of the transistors of said one conductivity type; and the drain extension well (182) of said one conductivity type of each of the

high-voltage transistors of said one conductivity type is formed by a s parate implantation of the opposite conductivity type into its w ll (174).

2. A proc ss according to claim 1, characterised in that the process further includes providing a thicker gate oxide layer selectively in the high-voltage transistors by growing a first oxide layer (88) both where the gates of the high-voltage transistors and the gates of the low-voltage transistors are to be provided, removing the first oxide layer (88) selectively where the gates of the low-voltage transistors are to be formed, and then growing a second oxide layer (389,489) where the first oxide layer was removed whilst simultaneously thickening the first oxide layer (189,289) where the gates of the high-voltage transistors are to be formed.

3. A process according to claim 1, characterised in that the common substrate (12) is of p-type conductivity and each of the transistors of said one conductivity type is formed in an n-type well (174,274,374), the n-type drain extension well (290) of each of the high-voltage transistors of the opposite conductivity type is formed by implantation and drive-in steps that also form said n-type wells (174,274,374) of the transistors of said one conductivity type, and the p-type extension well (182) of each high-voltage transistor of said one conductivity type is formed in a later selective implantation in a portion of its n-type well (174).

4. A process according to claim 1, for forming in a common substrate (12) NMOS and PMOS transistors that include lightly-doped drains and NMOS and PMOS transistors that are free of such lightly-doped drains, characterised in that the process comprises the steps of: forming spaced apart at a top surface (12a) of a monocrystalline silicon p-type substrate (12) a plurality of localized n-type wells (174,274,374), some of which are to form the PMOS transistors and others of which are to be used to form the drain extension wells (274) of the NMOS transistors that include lightly-doped regions; implanting with acceptor ions a first group of wells (174) of said plurality in which are to be formed the PMOS transistors with lightly-doped drains for use in forming the drain extension wells for said lightly-doped drains; and forming thick field regions (84,198,298) in said surface (12a) for defining the ends of the active surface regions of transistors to be formed at said surface (12a), thereby driving in said implanted acceptor ions to form the p-type extension wells (182) for the lightly-doped drains of the PMOS transistors that ar to include lightly-doped drains.

5. A process according to claim 4, characterised in that the process further comprises the step of implanting acceptor ions within sel ct d r gions of said p-type xtension wells (182) for forming heavily-doped drain regions (190) for said PMOS transistors with lightly-doped drains, whilst also implanting acc ptor ions into a s cond group of n-type wells (374) of said plurality to form the sources (390) and drains (392) of PMOS transistors that are free of lightly-doped drains.

6. A process according to claim 5, characterised in that the process further comprises the step of implanting donor ions into selected regions of a third group of n-type wells (274) of said plurality to form localized heavily-doped n-type drains (290) of NMOS transistors of the lightly-doped drain type, and into selected regions of the p-type substrate (12) to form the sources (492) and drains (490) of the NMOS transistors that are free of lightly-doped drains.

7. A process according to claim 6, characterised in that the process further comprises the steps of providing polysilicon gates (196,296, 396,496) to each of the transistors, and providing separate contacts to the source, drain and gate of the transistors formed in the substrate (12).

8. A process according to claim 1, for forming in a common substrate (12) PMOS transistors that include lightly-doped drains and that are free of lightly-doped drains and NMOS transistors that include lightly-doped drains and that are free of lightly-doped drains, characterised in that said process comprises the steps of: forming in a p-type substrate (12) by common processing a first group of n-type wells (174) to house PMOS transistors of the LDD type, a second group of the n-type wells (374) to house PMOS transistors which are not of the LDD type, and a third group of wells (274) to form drain extension regions of the NMOS transistors of the LDD type; forming in each of said first group of n-type wells (174) a p-type well (182) to form the drain extension region of a PMOS transistor of the LDD type; forming in common in each n-type well (174) of said first group of wells a p-type source (192) and within its p-type well (182) a p-type drain (190), and in each well (374) of said second group of n-type wells a p-type source (390) and a p-type drain (392); forming in common in each n-type well (274) of said third group of wells an n-type drain (290) and in the p-type substrate (12) an n-type region positioned to serve as the source (292) in co-operation with each n-type drain (290) of the third group to form an NMOS transistor of the LDD type and n-type regions (490,492) to co-operate as sources (492) and drains (490) of NMOS transistors not of the LDD type.

9. A process according to claim 1, of forming in a common substrat (12) an integrated circuit that includes both relatively low-voltage CMOS transistors and relatively high-voltage CMOS transistors of the LDD typ , characterised in that said proc ss compris s the steps of: forming at a sur-

face (12a) of a p-type substrate (12) a non-uniform layer of silicon oxide having relatively thick portions (170a,270a,370a,470a) and relatively thin portions (170b,270b,370b); irradiating the substrate with donor ions that are substantially blocked by the thick portions (170a,270a,370a,470a) of the oxide and that are implanted in substrate regions (171,271,371) underlying the thin portions (170b,270b,370b) of the oxide; heating the substrate (12) to drive the implanted donor ions deeper and forming n-type wells (174,274,374) in the substrate (12); removing the non-uniform layer of silicon oxide and re-growing a second layer (76) of uniform thickness; forming over said second layer surface a first masking layer that includes apertures overlying n-type wells (174) in which are selectively to be formed p-type wells (182) for serving as the lightly-doped drain extensions of the high-voltage PMOS transistors of the LDD type to be formed in the substrate (12); implanting acceptor ions into the selected n-type wells (174) through the apertures in the first masking layer; depositing over the second layer surface a layer of silicon nitride (178,278,378,478) that is apertured where field oxide regions are to be formed both for separating transistors laterally in the substrate and for supporting quasi-field plates in the high-voltage transistors; forming over the second layer surface a second masking layer (80) that is apertured except where the n-type wells (174,274,374) have been formed; implanting acceptor ions into the substrate (12) where not masked by the second masking layer (80) or by the silicon nitride (278,478) to provide a field implant that will underlie field oxide regions not overlying n-type wells (174,274,374); removing the second masking layer (80) from the second layer surface; heating the substrate (12) both to form field oxide regions (84,198,298,) where the substrate (12) is exposed in apertures in the silicon nitride layer and to drive-in the implanted acceptor ions for forming the p-type extension wells (182) in the selected n-type wells (174) where the high-voltage LDD PMOS transistors are to be formed; removing the silicon nitride layer (178,278,378,478) and the uniform silicon oxide layer (76) from the surface (12a) leaving the field oxide regions (84,198,298); growing a first gate oxide layer over the surface (12a) of the substrate (12) exposed between the field oxide regions (84,198,298); irradiating the surface (12a) of the substrate (12) with acceptor ions to set the surface potential of the substrate (12); forming over the surface (12a) of the substrate (12) a third masking layer (86) that is apertured where the low-voltage PMOS and CMOS transistors are to be formed; removing the first gate oxide layer where not masked by the third masking layer (86); r moving the third masking lay r (86); heating the substrate (12) to form a second gate oxide lay r (389,489) in active surface regions of the low-voltage transistors and to thicken the first gate oxide layer (189,289) in active surface regions of the high-voltage transistors; depositing a layer of polysilicon over the layered surface; thermally-doping the deposited polysilicon layer to increase its conductivity; patterning the polysilicon layer to define polysilicon gate electrodes (196,296,396,496) for the transistors; depositing a fourth masking layer over the surface; patterning the fourth masking layer to expose regions of the substrate where the sources (292,492) and drains (290,490) of the NMOS transistors are to be formed; irradiating the substrate (12) with donor ions to implant the sources (292,492) and drains (290,490) of the NMOS transistors; removing the fourth masking layer; depositing a fifth masking layer over the surface; patterning the fifth masking layer to expose regions of the substrate where the sources (192,390) and drains (190,392) of the PMOS transistors are to be formed; irradiating the surface to implant acceptor ions to form the sources (192,390) and drains (190,392) of the PMOS transistors; removing the fifth masking layer; and forming conductive contacts to the sources, drains and gate electrodes of the transistors.

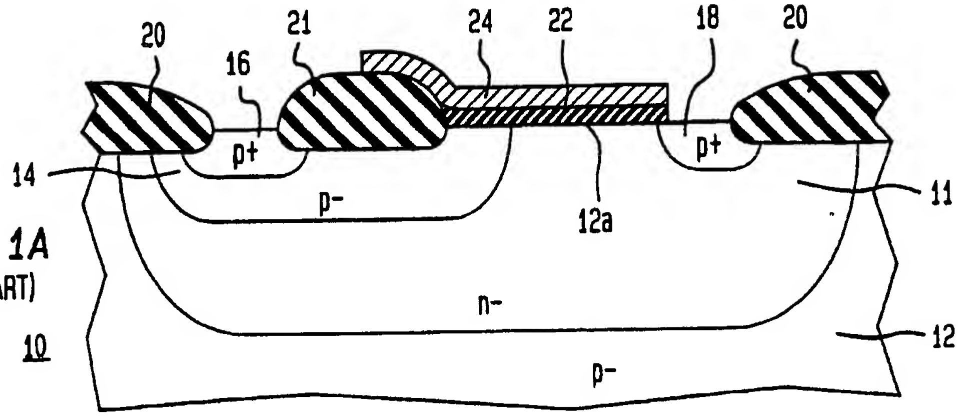



FIG. 1A
(PRIOR ART)

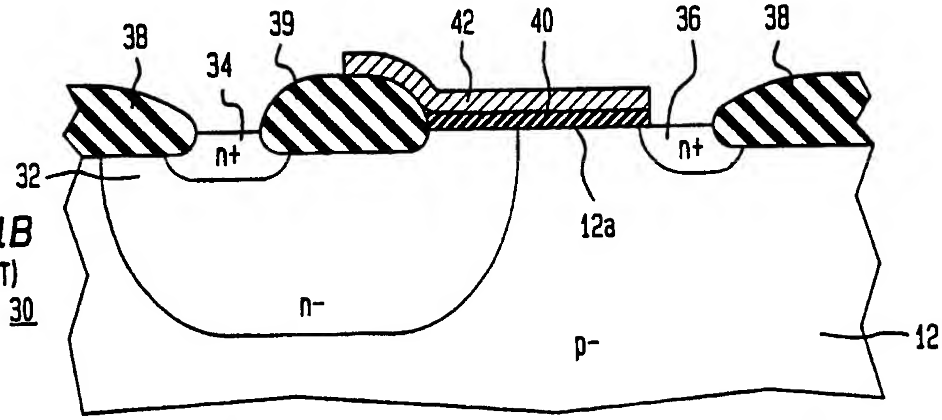



FIG. 1B
(PRIOR ART)

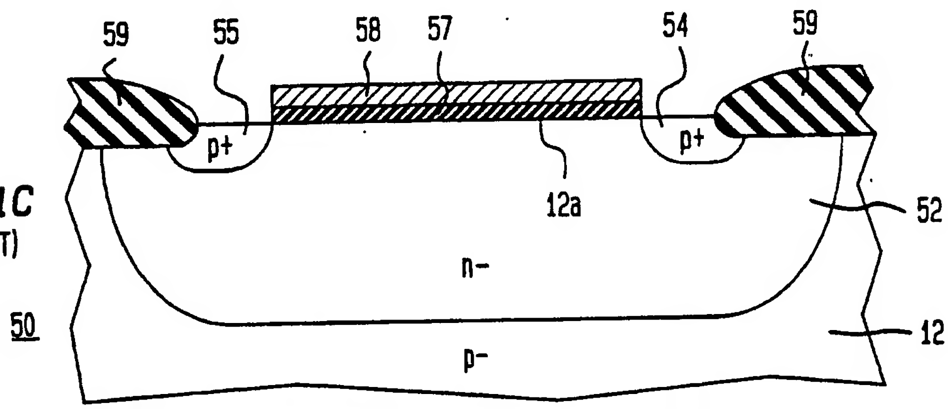



FIG. 1C
(PRIOR ART)

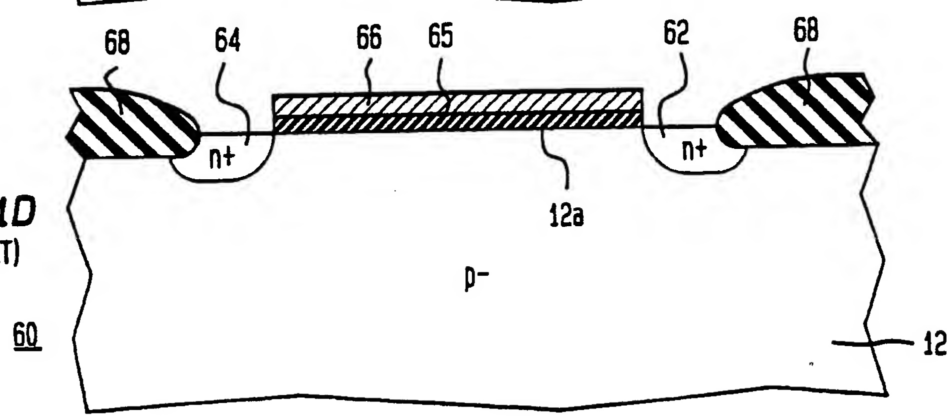



FIG. 1D
(PRIOR ART)

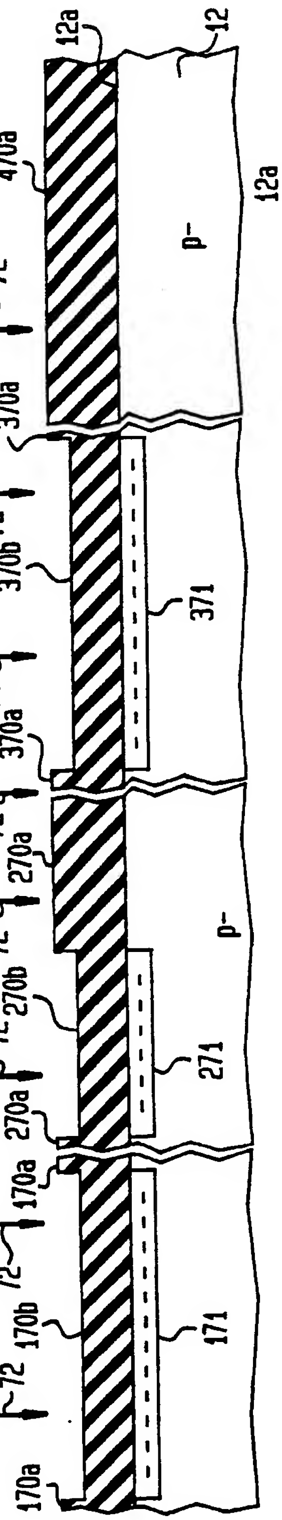



FIG. 2A

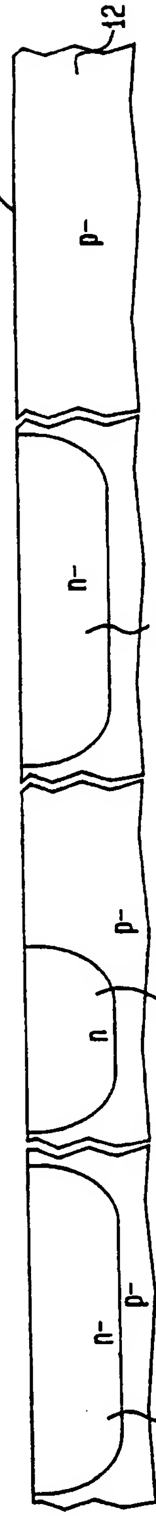



FIG. 2B

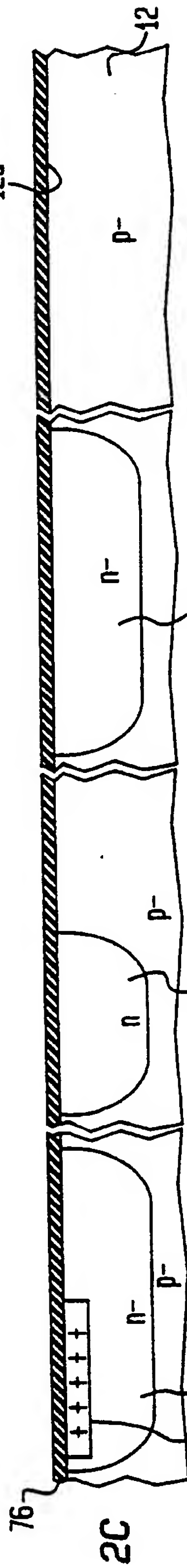



FIG. 2C

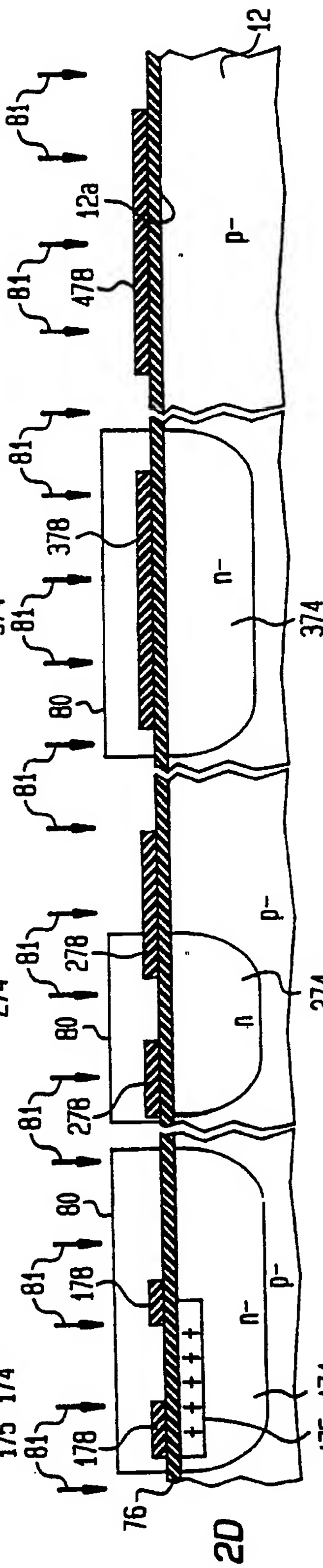



FIG. 2D

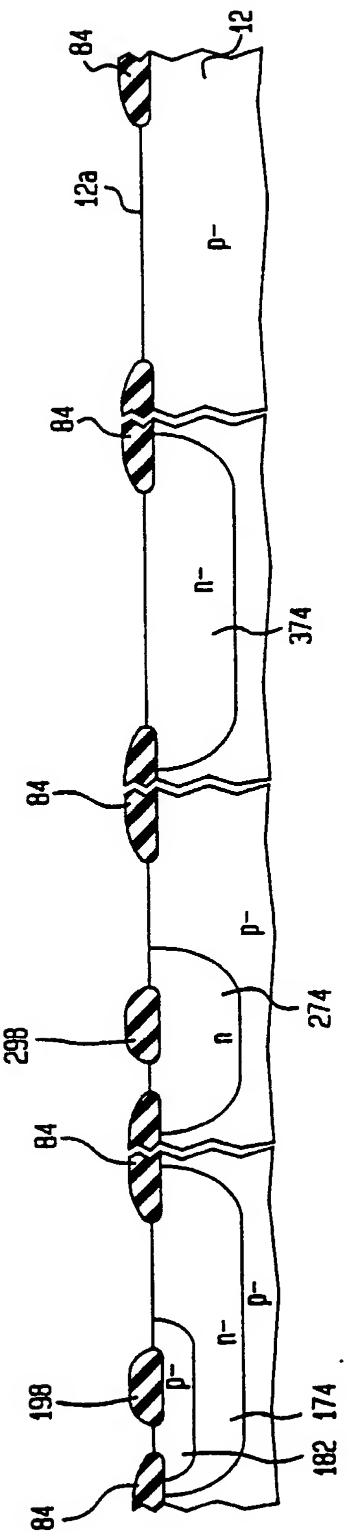
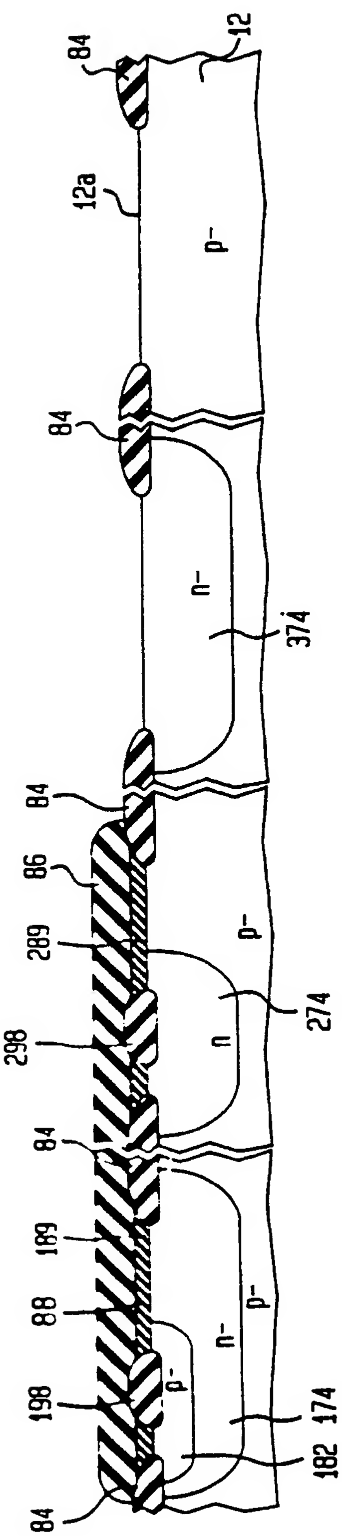

84
12
12a
p⁻
84
n⁻
374
84
p⁻
298
n
274
84
p⁻
n⁻
p⁻
198
84
182
174

FIG. 2E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189
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n⁻
p⁻
p⁻
198
174
182
84

FIG. 2F

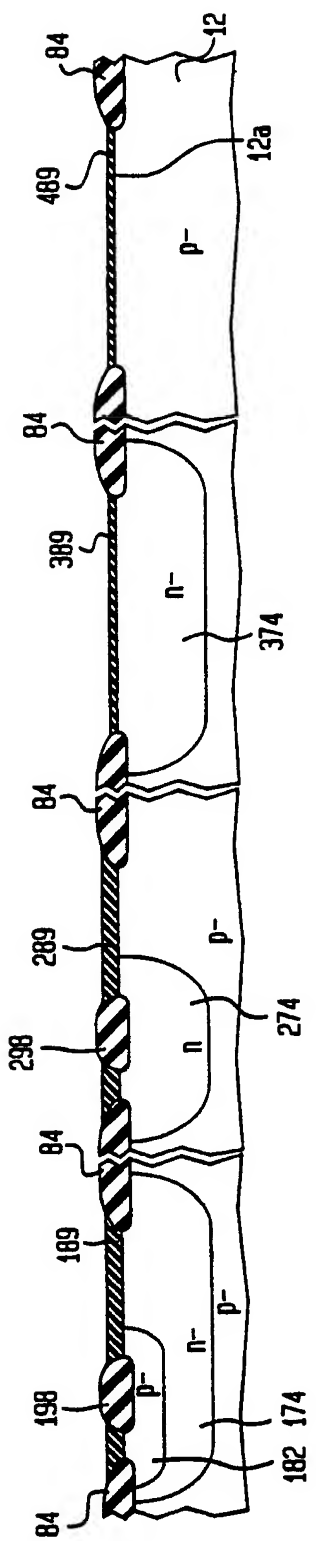


FIG. 2G

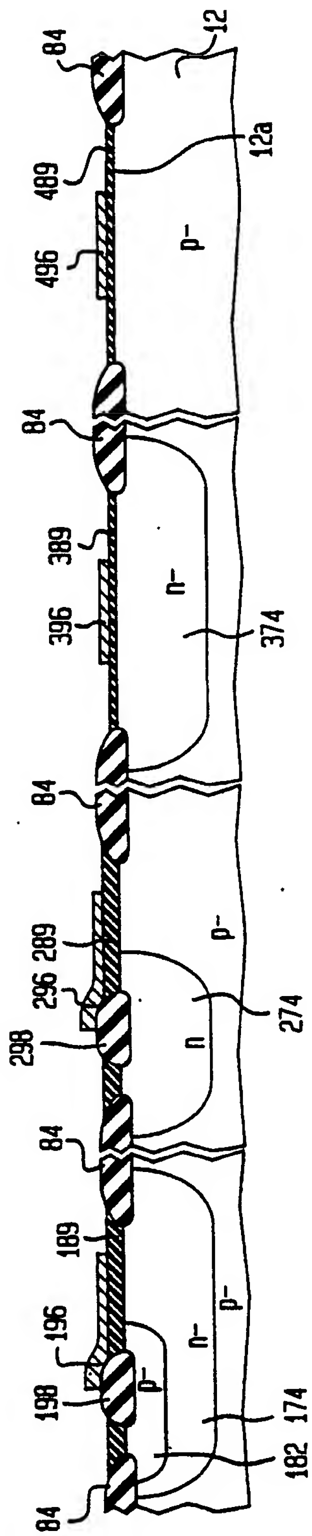


FIG. 2H

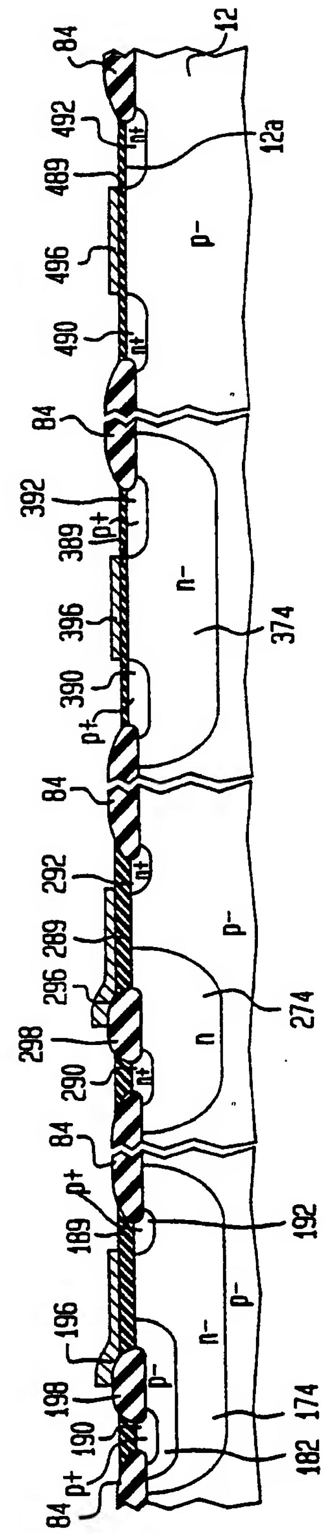


FIG. 2I

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(71) Applicant: **DELCO ELECTRONICS CORPORATION**
**700 East Firmin Street**
**Kokomo Indiana 46902(US)**

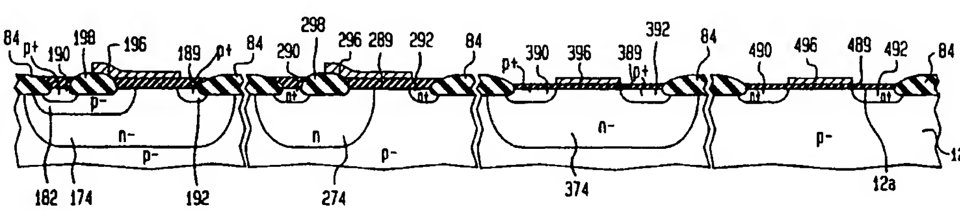
(72) Inventor: **Kosiak, Walter Kirk**
**2717 South Park Road**
**Kokomo, Indiana 46902(US)**
Inventor: **Mann, Jonathan Douglas**
**556 Kokomo Regency**
**Kokomo, Indiana 46902(US)**
Inventor: **Rowlands, Paul Russell, III**
**2204 Rouge Drive**
**Kokomo, Indiana 46902(US)**
Inventor: **Schnabel, Douglas Robert**
**3204 Woodbridge Circle**
**Kokomo, Indiana 46902(US)**
Inventor: **Parrish, Jack Duana**
**813 Williamsburg Drive**
**Kokomo, Indiana 46902(US)**

(74) Representative: **Haines, Arthur Donald et al**
**Patent Section 1st Floor Gideon House 28 Chapel Street**
**Luton, Bedfordshire LU1 2SE(GB)**

(54) **Process for forming high-voltage and low-voltage CMOS transistors on a single integrated circuit chip.**

(57) A process for forming both low-voltage CMOS transistors and high-voltage CMOS transistors on a common integrated circuit chip uses a common implantation and drive-in step to form both the n-type well (174,374) of each PMOS transistor and the n-type drain extension well (274) of each lightly-doped drain (LDD) NMOS transistor and a separate implant and drive-in to form the p-type drain extension well (182) of each LDD PMOS transistor.

FIG. 2I




EP 0 387 999 A3

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 90 30 1381

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| Y | EP-A-0 179 693 (THOMSON-CSF) * page 6, line 23 - page 12, line 22; figures 4-8 * | 1,3-9 | H01L21/84 H01L21/82 H01L29/08 |
| D,Y | IEEE TRANSACTIONS ON ELECTRON DEVICES vol. ED-33, no. 12, December 1986, NEW YORK USA pages 1985 - 1991; G.M. DOLNY ET AL.: 'enhanced cmos for analog-digital power ic applications' * page 1985, column 2 - page 1986, column 1; figures 1-3 * | 1,3-9 | |
| A | EP-A-0 157 926 (SIEMENS) * claims 1-9 * | 2 | |

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H01L

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| BERLIN | 19 MAY 1992 | JUHL A |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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